CLAIMS

What is claimed is:

1. A method for implementing a change to a circuit design for a system formed on a semiconductor chip, the circuit design including at least one circuit core, said method comprising:

providing in the circuit design at least one field programmable gate array (FPGA) core;

extracting an incremental change to the circuit design by comparing a new resister-transfer-level (RTL) design and an old RTL design for the system;

synthesizing said incremental change into a netlist for said at least one FPGA core;

generating new metal layer interconnections so as to provide an input and an output for said at least one FPGA core in accordance with said incremental change; and

programming said at least one FPGA core in accordance with the netlist.

2. A method according to claim 1, wherein said at least one FPGA core is provided in an otherwise unused area of the chip.

3. A method according to claim 1, wherein a plurality of FPGA cores are provided in an otherwise unused area of the chip, said plurality of FPGA core being interconnected by a bus.

4. A method according to claim 1, wherein said generating new metal interconnections includes:

locating nets to be an input for inputting an input signal to said at least one FPGA core;

changing metal layer interconnections so as to connect said input to said at least one FPGA core;

locating nets to be an output for receiving an output signal from said at least one FPGA core;

changing metal layer interconnections so as to connect said at least one FPGA core to said output; and

assigning an input/output interface of said FPGA core to said input and said output.

5. A method according to claim 1, further comprising:

providing in the circuit design backfill gates to be disposed in an otherwise unused area of the chip; and

selecting first backfill gates and second backfill gates for said at least one FPGA core based on said incremental change, said first backfill gates providing an input buffer for said at least one FPGA core, said second backfill gates providing an output buffer for said at least one FPGA core.

6. A method according to claim 5, wherein said generating new metal interconnections includes:

locating nets to be an input for inputting an input signal to said first backfill gates;

changing metal interconnections so as to connect said input to said first backfill gates, and to connect said first backfill gates to said at least one FPGA core;

locating nets to be an output for receiving an output signal from said second backfill gates;

changing metal interconnections so as to connect said at least one FPGA core to said second backfill gates, and to connect said second backfill gates to said output;

assigning a first configuration to said first backfill gates so as to provide said input signal to said at least one FPGA core;

assigning a second configuration to said second backfill gates so as to provide said output signal from said at least one FPGA core to said output; and

assigning an input/output interface of said FPGA core to said first backfill gates and said second backfill gates.

7. A method according to claim 1, further comprising:

running a first simulation with a system having the new RTL design;

running a second simulation with a system having the old RTL design with said incremental change;

comparing results of the first simulation and the second simulation; and

revising, if necessary, the new metal layer interconnections based on said comparing.

8. A method according to claim 1, further comprising:

performing a metalization process for the new metal layers on a wafer, thereby forming said new metal layer interconnections on the wafer, the wafer including a substrate having a same semiconductor structure as a substrate adapted to a system having the old RTL design.

9. A method according to claim 8, further comprising:

configuring said at least one FPGA core embedded in each chip in accordance with said programming.

10. A method according to claim 1, wherein said circuit design of a system formed on a chip includes at least one of an application specific integrated circuit (ASIC) design and an application specific standard product (ASSP) design.

11. A system formed on a semiconductor chip, a circuit design for said system including an incremental change from an old circuit design, said system comprising:

at least one circuit core provided on a semiconductor substrate;

at least one field programmable gate array (FPGA) core, said at least one FPGA core being programmed and configured to reflect the incremental change; and

metal layers formed on the semiconductor substrate, said metal layer having interconnections providing an input and an output for said at least one FPGA core in accordance with the incremental change.

Replacement Page

12. A system according to claim 11, wherein said at least one FPGA core is provided in an otherwise unused area of the chip.

13. A system according to claim 11, wherein a plurality of FPGA cores are provided in an otherwise unused area of the chip, said plurality of FPGA core being interconnected by a bus.

14. A system according to claim 11, wherein said FPGA core includes an input-output interface, said metal layer interconnections including:

a first connection between said input and said input/output interface; and

a second connection between said output and said input/output interface.

15. A system according to claim 11, further comprising:

backfill gates disposed in an otherwise unused area of the semiconductor substrate, first backfill gates and second backfill gates being selected to be used with said at least one FPGA core.

16. A system according to claim 15, wherein said first backfill gates provide an input buffer for said at least one FPGA, and said second backfill gates provides an output buffer for said at least one FPGA core.

17. A system according to claim 15, wherein said FPGA core includes an input-output interface, said metal layer interconnections including:

a first connection from said input through said first backfill gates to said input/output interface; and

a second connection from said input/output interface through said second backfill gates to said output.

18. A system according to claim 11, wherein said incremental change includes a difference between a new resister-transfer-level (RTL) design and an old RTL design for said system.

19. A system according to claim 18, wherein said at least one FPGA core implements a netlist synthesized from said incremental change.

20. A system according to claim 11, wherein said system formed on a chip includes at least one of an application specific integrated circuit (ASIC) and an application specific standard product (ASSP).

21. An apparatus for implementing a change to a circuit design for a system formed on a semiconductor chip, the circuit design including at least one circuit core, said apparatus comprising:

means for providing in the circuit design at least one field programmable gate array (FPGA) core to be placed in an unused area of the chip;

means for extracting an incremental change to the circuit design by comparing a new resister-transfer-level (RTL) design and an old RTL design for the system;

means for synthesizing said incremental change into a netlist for said at least one FPGA core;

means for generating new metal layer interconnections so as to provide an input and an output for said at least one FPGA core in accordance with said incremental change; and

means for programming said at least one FPGA core in accordance with the netlist.

22. An apparatus according to claim 21, wherein said at least one FPGA core is provided in an otherwise unused area of the chip.

23. An apparatus according to claim 21, wherein a plurality of FPGA cores are provided in an otherwise unused area of the chip, said plurality of FPGA core being interconnected by a bus.

24. An apparatus according to claim 21, wherein said means for generating new metal interconnections includes:

means for locating nets to be an input for inputting an input signal to said at least one FPGA core;

means for changing metal layer interconnections so as to connect said input to said at least one FPGA core;

means for locating nets to be an output for receiving an output signal from said at least one FPGA core;

means for changing metal layer interconnections so as to connect said at least one FPGA core to said output; and

means for assigning an input/output interface of said FPGA core to said input and said output.

25. An apparatus according to claim 21, further comprising:

means for providing in the circuit design backfill gates to be disposed in an otherwise unused area of the chip; and

means for selecting first backfill gates and second backfill gates for said at least one FPGA core based on said incremental change, said first backfill gates providing an input buffer for said at least one FPGA, said second backfill gates providing an output buffer for said at least one FPGA core.

26. An apparatus according to claim 25, wherein said means for generating new metal interconnections includes:

means for locating nets to be an input for inputting an input signal to said first backfill gates;

means for changing metal interconnections so as to connect said input to said first backfill gates, and to connect said first backfill gates to said at least one FPGA core;

means for locating nets to be an output for receiving an output signal from said second backfill gates;

means for changing metal interconnections so as to connect said at least one FPGA core to said second backfill gates, and to connect said second backfill gates to said output;

means for assigning a first configuration to said first backfill gates so as to provide said input signal to said at least one FPGA core;

means for assigning a second configuration to said second backfill gates so as to provide said output signal from said at least one FPGA core to said output; and

means for assigning an input/output interface of said FPGA core to said first backfill gates and said second backfill gates.

27. An apparatus according to claim 21, further comprising:

means for running a first simulation with a system having the new RTL design;

means for running a second simulation with a system having the old RTL design with said incremental change;

means for comparing results of the first simulation and the second simulation; and

means for revising, if necessary, the new metal layer interconnections based on said comparing.

28. An apparatus according to claim 21, further comprising:

means for performing a metalization process for the new metal layers on a wafer, thereby forming said new metal layer interconnections on the wafer, the wafer having a same semiconductor structure as a wafer for a system having the old RTL design.

29. An apparatus according to claim 28, further comprising:

means for configuring said at least one FPGA core embedded in each chip in accordance with said programming.

30. An apparatus according to claim 21, wherein said circuit design of a system formed on a chip includes at least one of an application specific integrated circuit (ASIC) design and an application specific standard product (ASSP) design.

31. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for implementing a change to a circuit design for a system formed on a semiconductor chip, the circuit design including at least one circuit core, said method comprising:

providing in the circuit design at least one field programmable gate array (FPGA) core to be placed in an unused area of the chip;

extracting an incremental change to the circuit design by comparing a new resister-transfer-level (RTL) design and an old RTL design for the system;

synthesizing said incremental change into a netlist for said at least one FPGA core;

generating new metal layer interconnections so as to provide an input and an output for said at least one FPGA core in accordance with said incremental change; and

programming said at least one FPGA core in accordance with the netlist.

32. A program storage device according to claim 31, wherein said generating new metal interconnections includes:

locating nets to be an input for inputting an input signal to said at least one FPGA core;

changing metal layer interconnections so as to connect said input to said at least one FPGA core;

locating nets to be an output for receiving an output signal from said at least one FPGA core;

changing metal layer interconnections so as to connect said at least one FPGA core to said output; and

assigning an input/output interface of said FPGA core to said input and said output.

33. A program storage device according to claim 31, wherein said method further comprises:

providing in the circuit design backfill gates to be disposed in an otherwise unused area of the chip; and

selecting first backfill gates and second backfill gates for said at least one FPGA core based on said incremental change, said first backfill gates providing an input buffer for said at least one FPGA, said second backfill gates providing an output buffer for said at least one FPGA core.

Express Mail Label No.

34. A program storage device according to claim 33, wherein said generating new metal interconnections includes:

locating nets to be an input for inputting an input signal to said first backfill gates;

changing metal interconnections so as to connect said input to said first backfill gates, and to connect said first backfill gates to said at least one FPGA core;

locating nets to be an output for receiving an output signal from said second backfill gates;

changing metal interconnections so as to connect said at least one FPGA core to said second backfill gates, and to connect said second backfill gates to said output;

assigning a first configuration to said first backfill gates so as to provide said input signal to said at least one FPGA core;

assigning a second configuration to said second backfill gates so as to provide said output signal from said at least one FPGA core to said output; and

assigning an input/output interface of said FPGA core to said first backfill gates and said second backfill gates.

35. A program storage device according to claim 31, wherein said method further comprises:

running a first simulation with a system having the new RTL design;

running a second simulation with a system having the old RTL design with said incremental change;

comparing results of the first simulation and the second simulation; and

revising, if necessary, the new metal layer interconnections based on said comparing.

Express Mail Label No.